Amendments to the Specification:

Please add the following new paragraph after paragraph [0077]:

[0077.1] FIGS. 54A-C illustrate Ensemble Multiply Add instructions in accordance with an exemplary embodiment of the present invention.

Please add the following new paragraph after paragraph [0236]:

[0236.1] Ensemble Multiply-Add

[0236.2] FIG. 54A present various examples of Ensemble Multiply Add instructions. FIGS. 54B-C illustrate an exemplary embodiment of formats and operation codes that can be used to perform the various Ensemble Multiply Add instructions. In these examples, Ensemble Multiply Add instructions have been labeled as "EnsembleInplace." As shown in FIGS. 54B-C, in this exemplary embodiment, operations take operands from three registers, perform operations on partitions of bits in the operands, and place the concatenated results in the third register. Specifically, the contents of registers rd, rc and rb are partitioned into groups of operands of the size specified, and for each partitioned element, the contents of registers rc and rb are multiplied and added to the contents of register rd, yielding a group of results. The group of results is catenated and placed in register rd. Register rd is both a source and destination of this instruction.